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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Steven L. Pline, et al.	Examiner:	Charles Ehne
Serial No.:	10/725,855	Group Art Unit:	2113
Filed:	December 2, 2003	Docket No.:	10014281-1
Title:	DATA STORAGE SYSTEM WITH ERROR CORRECTION CODE AND REPLACEABLE DEFECTIVE MEMORY		

CERTIFICATE OF TRANSMISSION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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1. Transmittal of Appeal Brief (1 pg.); and
2. Appeal Brief Under 37 C.F.R. 41.37 (23 pgs.).

Date: April 24, 2007

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By: Steven E. Dicke

Name: Steven E. Dicke (Reg. No. 38,431)

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HEWLETT-PACKARD COMPANY
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PATENT APPLICATION

ATTORNEY DOCKET NO. 10014281-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Steven L. Pline, et al.

Confirmation No.: 3242

Application No.: 10/725,855

Examiner: Charles Ehne

Filing Date: December 2, 2003

Group Art Unit: 2113

Title: DATA STORAGE SYSTEM WITH ERROR CORRECTION CODE AND REPLACEABLE DEFECTIVE MEMORY

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on February 2, 2007.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☒ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☒ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☐ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 620. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Date of facsimile: April 24, 2007
Typed Name: Steven E. Dicke
Signature: Steven E. Dicke

Respectfully submitted,
Steven L. Pline, et al.
By Steven E. Dicke
Steven E. Dicke
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Rev 10/05 (ApiBrief)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Steven L. Pline, et al.	Examiner:	Charles Ehne
Serial No.:	10/725,855	Group Art Unit:	2113
Filed:	December 2, 2003	Docket No.:	10014281-1
Due Date:	**April 2, 2007**		
Title:	DATA STORAGE SYSTEM WITH ERROR CORRECTION CODE AND REPLACEABLE DEFECTIVE MEMORY		

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on February 2, 2007, appealing the final rejection of claims 1-35 of the above-identified application as set forth in the Final Office Action mailed November 2, 2006.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. §41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-35.

Appeal Brief to the Board of Patent Appeals and Interferences
Applicant: Steven L. Pline, et al.
Serial No.: 10/725,855
Filed: December 2, 2003
Docket No.: 10014281-1
Title: DATA STORAGE SYSTEM WITH ERROR CORRECTION CODE AND REPLACEABLE DEFECTIVE MEMORY

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REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed November 2, 2006, claims 1-35 were finally rejected. Claims 1-35 are pending in the application, and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed November 2, 2006.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The Summary is set forth as an exemplary embodiment as the language corresponding to independent claims 1, 13, 23, 29, and 33. Discussions about elements of claims 1, 13, 23, 29, and 33 can be found at least at the cited locations in the specification and drawings.

The present invention, as claimed in independent claim 1, provides a data storage and retrieval system operating on a host computer (22). The data storage and retrieval system includes a sparing system (38) configured to replace defective memory sections of a memory device (24) with replacement memory sections of the memory device (24). The sparing system (38) includes computer readable instructions stored in a host memory (28) of the host computer (22). The data storage and retrieval system includes an error correction code

system (40) configured to encode data with an error correction code, store the data into the memory device (24), and decode the encoded data with the error correction code to retrieve the data from the memory device (24). The error correction code system (40) includes computer readable instructions stored in the host memory (28) of the host computer (22). (See, e.g., specification, paragraph 0021 through paragraph 0046; and Figure 1).

The present invention, as claimed in independent claim 13, provides a host computer (22). The host computer (22) includes a host memory (28) storing instructions (40, 38) to provide an error correction code and to replace defective memory sections of a storage device (24) with spare memory sections of the storage device (24). The host computer (22) includes a host processor (26) that executes the instructions (40, 38) to encode and decode data stored in the storage device (24) with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections. The addresses of the spare memory sections are provided to the storage device (24) during data transfers between the storage device (24) and the host computer (22). (See, e.g., specification, paragraph 0021 through paragraph 0046; and Figure 1).

The present invention, as claimed in independent claim 23, provides a host computer system (22). The host computer system (22) includes means (40) for correcting errors in data retrieved from a storage style memory device (24). The means (40) for correcting errors includes computer readable instructions (40) stored in a host memory (28) of the host computer system (22). The host computer system (22) includes means (38) for identifying defective sections of memory in the storage style memory device (24). The defective sections of memory provide more errors than a predetermined threshold value. The host computer system (22) includes means (38) for sparing the defective sections of memory with replacement sections of memory in the storage style memory device (24). The means (38) for sparing includes computer readable instructions (38) stored in the host memory (28) of the host computer system (22). (See, e.g., specification, paragraph 0021 through paragraph 0046; and Figure 1).

The present invention, as claimed in independent claim 29, provides a method for storing and retrieving data. The method includes providing a host computer (22) and a memory device (24) and providing computer-executable sparing instructions (38) and error

correction code instructions (40). The method includes replacing addresses for defective memory sections in a memory device (24) with addresses for replacement memory sections in the memory device (24) by executing the sparing instructions (38) on the host computer (22). The method includes providing the addresses for the replacement memory sections to the memory device (24) during read and write operations with the memory device (24) by executing the sparing instructions (38) on the host computer (22). The method includes encoding original data with an error correction code to write encoded data into the memory device (24) by executing the error correction code instructions (40) on the host computer (22). The method includes decoding data retrieved from a selected memory section of the memory device (24) with the error correction code by executing the error correction code instructions (40) on the host computer (22). (See, e.g., specification, paragraph 0021 through paragraph 0046; and Figure 1).

The present invention, as claimed in independent claim 33, provides a method for storing and retrieving data. The method includes providing a host computer (22) and a storage style memory device (24) and providing computer-executable sparing instructions (38) and error correction code instructions (40). The method includes sparing out sections of memory in the storage style memory device (24) by executing the sparing instructions (38) on the host computer (22). The method includes encoding and decoding data stored in the storage style memory device (24) with an error correction code by executing the error correction code instructions (40) on the host computer (22). (See, e.g., specification, paragraph 0021 through paragraph 0046; and Figure 1).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1-8, 10, 11, 13-17, 23, and 26-35 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Hiratsuka, U.S. Patent No. 6,119,245 ("Hiratsuka").

II. Claim 12 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Martyn Riley (non patent literature).

III. Claim 9 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Weng et al., U.S. Patent No. 5,428,630 ("Weng").

IV. Claims 18, 19, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Tsunoda et al., U.S. Patent Pub. No. 2003/0028733 ("Tsunoda").

V. Claims 21 and 22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Kleveland et al., U.S. Patent Pub. No. 2003/0115518 ("Kleveland").

VI. Claims 24 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Buternowsky et al., U.S. Patent No. 5,809,090 ("Buternowsky").

ARGUMENT

I. The Applicable Law

"A claim is anticipated if each and every element as set forth in the claim is found, either expressly or inherently described, in a single, prior art reference." *Verdegaal Bros. v. Union Oil Co., of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner has the burden under 35 U.S.C. §103 to establish a *prima facie* case of obviousness. *In re Fine,* 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *Id.* Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Third, the prior art reference or combined prior art references must teach or suggest all of the claim limitations. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974). These three criteria are also set forth in §706.02(j) of the M.P.E.P.

II. Rejection of Claims 1-8, 10, 11, 13-17, 23, and 26-35 under 35 U.S.C. §102(b) as being unpatentable over Hiratsuka

The Examiner rejected claims 1-8, 10, 11, 13-17, 23, and 26-35 under 35 U.S.C. § 102(b) as being unpatentable over Hiratsuka, U.S. Patent No. 6,119,245 ("Hiratsuka"). Appellants respectfully submit that Hiratsuka does not teach or suggest the invention of independent claims 1, 13, 23, 29, and 33, and the claims depending therefrom.

A. Rejection of Claims 1-8, 10, and 11 under 35 U.S.C. §102(b) as being unpatentable over Hiratsuka

Independent claim 1 recites **a data storage and retrieval system operating on a host computer, the sparing system comprising computer readable instructions stored in a host memory of the host computer** and **the error correction code system comprising computer readable instructions stored in the host memory of the host computer**.

Hiratsuka discloses a semiconductor disk device 100 including a flash memory section 110, a disk controller section 120, and a microcontroller section 130. (Col. 5, lines 9-11; and Fig. 1). Disk controller section 120 includes a host interface 121 for transferring address information and/or command information or main data etc. with the outside of semiconductor disk device 100. Disk controller section 120 also includes micro CPU interface 122 for transferring address information and/or command information or control signals etc. with respect to disk controller section 120 and microcontroller section 130. (Col. 5, lines 20-27; and Fig. 1). Micro CPU 131 in microcontroller section 130 controls flash memory section 110 and disk controller section 120 in accordance with the command information and/or address information etc. that is input from outside through host interface 121 and micro CPU interface 122. (Col. 6, lines 25-29).

Hiratsuka further discloses that ECC control section 126, on data writing, fetches write data from flash memory interface 125 and compiles ECC data, which it then sends to flash memory interface 125. Also, when data is read, it performs an operation of inputting main data and ECC data from flash memory interface 125 and detecting whether or not a data error has been generated and/or an operation of correcting main data if generation of a COR is detected. (Col. 5, lines 46-53). Data error information management table 127 stores for

each sector of memory elements M(0)-M(9) the number of times of occurrence of data errors. (Col. 5, lines 54-56). Address conversion table 128 converts memory numbers in address information that is input from the external host computer into physical memory numbers and output. (Col. 6, lines 16-19).

Hiratsuka discloses a disk controller including hardware components that provide ECC encoding and decoding, data error information management, and address conversion. The disk controller includes a host interface 121 for communicating with a host computer. The host computer in Hiratsuka does not perform any of the error correction, data error information management, or address conversion functions. The host computer in Hiratsuka provides command information and address information to semiconductor device 100 through host interface 121. (Col. 6, lines 40-43). Determination of whether or not address conversion is to be performed and rewriting of logical memory numbers are performed by micro CPU 131. (Col. 6, lines 21-24). Micro CPU 131 uses conversion table 128, which is part of disk controller section 120, to perform address conversion. (See col. 6, lines 51-60). ECC control section 126, which is part of disk controller section 120, compiles the ECC data. (See col. 6, lines 63-67). Both the address conversion and ECC functions disclosed by Hiratsuka are performed independently from the host computer and without the host computer's knowledge. The host computer just reads and writes data to the memory device 100 without being involved in the address conversion or ECC functions.

In contrast, claim 1 recites a system that operates on a *host computer*. In addition, the sparing system and the error correction code system comprise *computer readable instructions* stored in a *host memory* of the *host computer*. The sparing system and the error correction code system recited by claim 1 are implemented using computer readable instructions executed on the host computer. The host computer performs the sparing and ECC functions. The memory device recited by claim 1 has no knowledge or control of the sparing system or the ECC system. In contrast, Hiratsuka discloses address conversion and ECC functions that are performed by the storage device without knowledge or control by the host computer.

In view of the above, independent claim 1 is not taught or suggested by Hiratsuka. Appellants submit that independent claim 1 is not anticipated by Hiratsuka, and respectfully request that the rejection of independent claim 1 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claims 2-8, 10, and 11, which further define patentably distinct independent claim 1, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 2-8, 10, and 11 are not anticipated by Hiratsuka, and respectfully request that the rejection of dependent claims 2-8, 10, and 11 under 35 U.S.C. § 102(b) be withdrawn.

B. Rejection of Claims 13-17 under 35 U.S.C. §102(b) as being unpatentable over Hiratsuka

Independent claim 13 recites **a host computer comprising host memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a host processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections.** For at least the reasons set forth above with respect to claim 1, Hiratsuka does not teach or suggest the above-quoted limitations of claim 13.

In view of the above, independent claim 13 is not taught or suggested by Hiratsuka. Appellants submit that independent claim 13 is not anticipated by Hiratsuka, and respectfully request that the rejection of independent claim 13 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claims 14-17, which further define patentably distinct independent claim 13, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 14-17 are not anticipated by Hiratsuka, and respectfully request that the rejection of dependent claims 14-17 under 35 U.S.C. § 102(b) be withdrawn.

C. Rejection of Claims 23 and 26-28 under 35 U.S.C. §102(b) as being unpatentable over Hiratsuka

Independent claim 23 recites **a host computer system comprising means for correcting errors in data retrieved from a storage style memory device, the means for correcting errors comprising computer readable instructions stored in a host memory of the host computer system; and means for sparing the defective sections of memory**

with replacement sections of memory in the storage style memory device, the means for sparing comprising computer readable instructions stored in the host memory of the host computer system. For at least the reasons set forth above with respect to claim 1, Hiratsuka does not teach or suggest the above-quoted limitations of claim 23.

In view of the above, independent claim 23 is not taught or suggested by Hiratsuka. Appellants submit that independent claim 23 is not anticipated by Hiratsuka, and respectfully request that the rejection of independent claim 23 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claims 26-28, which further define patentably distinct independent claim 23, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 26-28 are not anticipated by Hiratsuka, and respectfully request that the rejection of dependent claims 26-28 under 35 U.S.C. § 102(b) be withdrawn.

D. Rejection of Claims 29-32 under 35 U.S.C. §102(b) as being unpatentable over Hiratsuka

Independent claim 29 recites **providing computer-executable sparing instructions and error correction code instructions; replacing addresses for defective memory sections in a memory device with addresses for replacement memory sections in the memory device by executing the sparing instructions on the host computer; providing the addresses for the replacement memory sections to the memory device during read and write operations with the memory device by executing the sparing instructions on the host computer; encoding original data with an error correction code to write encoded data into the memory device by executing the error correction code instructions on the host computer; and decoding data retrieved from a selected memory section of the memory device with the error correction code by executing the error correction code instructions on the host computer.** For at least the reasons set forth above with respect to claim 1, Hiratsuka does not teach or suggest the above-quoted limitations of claim 29.

In view of the above, independent claim 29 is not taught or suggested by Hiratsuka. Appellants submit that independent claim 29 is not anticipated by Hiratsuka, and respectfully request that the rejection of independent claim 29 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claims 30-32, which further define patentably distinct independent claim 29, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 30-32 are not anticipated by Hiratsuka, and respectfully request that the rejection of dependent claims 30-32 under 35 U.S.C. § 102(b) be withdrawn.

E. Rejection of Claims 33-35 under 35 U.S.C. §102(b) as being unpatentable over Hiratsuka

Independent claim 33 recites **providing computer-executable sparing instructions and error correction code instructions; sparing out sections of memory in the storage style memory device by executing the sparing instructions on the host computer; and encoding and decoding data stored in the storage style memory device with an error correction code by executing the error correction code instructions on the host computer.** For at least the reasons set forth above with respect to claim 1, Hiratsuka does not teach or suggest the above-quoted limitations of claim 33.

In view of the above, independent claim 33 is not taught or suggested by Hiratsuka. Appellants submit that independent claim 33 is not anticipated by Hiratsuka, and respectfully request that the rejection of independent claim 33 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claims 34 and 35, which further define patentably distinct independent claim 3, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 34 and 35 are not anticipated by Hiratsuka, and respectfully request that the rejection of dependent claims 34 and 35 under 35 U.S.C. § 102(b) be withdrawn.

III. Rejection of Claim 12 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Martyn Riley

The Examiner rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Martyn Riley. Appellants submit that the Examiner has not established a case of *prima facie* obviousness of claim 12.

Dependent claim 12 is dependent on independent claim 1. As described above with respect to independent claim 1, Hiratsuka does not teach or suggest each and every limitation of this independent claim. Dependent claim 12 further defines patentably distinct

independent claim 1, is further distinguishable over the cited references, and is believed to be allowable over the cited references. The Examiner has not established a *prima facie* case of obviousness of claim 12, and Appellants respectfully request that the rejection of dependent claim 12 under 35 U.S.C. § 103(a) be withdrawn.

IV. Rejection of Claim 9 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Weng

The Examiner rejected claim 9 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Weng et al., U.S. Patent No. 5,428,630 ("Weng"). Appellants submit that the Examiner has not established a case of *prima facie* obviousness of claim 9.

Dependent claim 9 is dependent on independent claim 1. As described above with respect to independent claim 1, Hiratsuka does not teach or suggest each and every limitation of this independent claim. Dependent claim 9 further defines patentably distinct independent claim 1, is further distinguishable over the cited references, and is believed to be allowable over the cited references. The Examiner has not established a *prima facie* case of obviousness of claim 9, and Appellants respectfully request that the rejection of dependent claim 9 under 35 U.S.C. § 103(a) be withdrawn.

V. Rejection of Claims 18, 19, and 20 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Tsunoda

The Examiner rejected claims 18, 19, and 20 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Tsunoda et al., U.S. Patent Pub. No. 2003/0028733 ("Tsunoda"). Appellants submit that the Examiner has not established a case of *prima facie* obviousness of claims 18, 19, and 20.

Dependent claims 18, 19, and 20 are dependent on independent claim 13. As described above with respect to independent claim 13, Hiratsuka does not teach or suggest each and every limitation of this independent claim. Dependent claims 18, 19, and 20 further define patentably distinct independent claim 13, are further distinguishable over the cited references, and are believed to be allowable over the cited references. The Examiner has not established a *prima facie* case of obviousness of claims 18, 19, and 20, and Appellants

respectfully request that the rejection of dependent claims 18, 19, and 20 under 35 U.S.C. § 103(a) be withdrawn.

VI. Rejection of Claims 21 and 22 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Kleveland

The Examiner rejected claims 21 and 22 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Kleveland et al., U.S. Patent Pub. No. 2003/0115518 ("Kleveland"). Appellants submit that the Examiner has not established a case of *prima facie* obviousness of claims 21 and 22.

Dependent claims 21 and 22 are dependent on independent claim 13. As described above with respect to independent claim 13, Hiratsuka does not teach or suggest each and every limitation of this independent claim. Dependent claims 21 and 22 further define patentably distinct independent claim 13, are further distinguishable over the cited references, and are believed to be allowable over the cited references. The Examiner has not established a *prima facie* case of obviousness of claims 21 and 22, and Appellants respectfully request that the rejection of dependent claims 21 and 22 under 35 U.S.C. § 103(a) be withdrawn.

VII. Rejection of Claims 24 and 25 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Buternowsky

The Examiner rejected claims 24 and 25 under 35 U.S.C. §103(a) as being unpatentable over Hiratsuka in view of Buternowsky et al., U.S. Patent No. 5,809,090 ("Buternowsky"). Appellants submit that the Examiner has not established a case of *prima facie* obviousness of claims 24 and 25.

Dependent claims 24 and 25 are dependent on independent claim 23. As described above with respect to independent claim 23, Hiratsuka does not teach or suggest each and every limitation of this independent claim. Dependent claims 24 and 25 further define patentably distinct independent claim 23, are further distinguishable over the cited references, and are believed to be allowable over the cited references. The Examiner has not established a *prima facie* case of obviousness of claims 24 and 25, and Appellants respectfully request that the rejection of dependent claims 24 and 25 under 35 U.S.C. § 103(a) be withdrawn.

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CONCLUSION

For the above reasons, Appellants respectfully submit that the cited references neither anticipate nor render obvious claims of the pending Application. The pending claims distinguish over the cited references, and therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-35 be allowed.

Any inquiry regarding this Response should be directed to either Brian R. Short at Telephone No. (408) 888-9830, Facsimile No. (650) 852-8063 or Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

IP Administration
Legal Department, M/S 35
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Respectfully submitted,

Steven L. Pline, et al.,

By their attorneys,

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Dated: April 24, 2007
SED:kmh

Steven E. Dicke
Reg. No. 38,431

CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via telefacsimile to Fax No. (571) 273-8300 on this 24th day of April, 2007.

By: Steven E. Dicke
Name: Steven E. Dicke

CLAIMS APPENDIX

1. (Previously Presented) A data storage and retrieval system operating on a host computer, the data storage and retrieval system comprising:

a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device, the sparing system comprising computer readable instructions stored in a host memory of the host computer; and

an error correction code system configured to encode data with an error correction code, store the data into the memory device, and decode the encoded data with the error correction code to retrieve the data from the memory device, the error correction code system comprising computer readable instructions stored in the host memory of the host computer.

2. (Previously Presented) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table stored in the host memory.

3. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table stored in the memory device.

4. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table comprising entries obtained from a tester that tests the memory device.

5. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table comprising entries obtained from the sparing system that is configured to test the memory device to obtain the entries for the sparing table.

6. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table, and the sparing system and the error correction code system are configured to update the sparing table as defective memory sections are detected in the memory device.

7. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table and the error correction code system is configured to detect defective memory sections in the memory device, and the sparing system is configured to update the sparing table with address locations of the detected defective memory sections in the memory device.

8. (Original) The data storage and retrieval system of claim 7, where the error correction code system is configured to correct errors in a selected memory section of the memory device, count the errors to obtain an error count and compare the error count to a threshold value to establish if the selected memory section is defective.

9. (Original) The data storage and retrieval system of claim 8, where the threshold value is greater than 50% of a power of the error correction code.

10. (Original) The data storage and retrieval system of claim 1, where the error correction code system is configured to encode and decode all data stored in the memory device.

11. (Original) The data storage and retrieval system of claim 1, where the error correction code system is configured to encode and decode selected data stored in the memory device.

12. (Original) The data storage and retrieval system of claim 1, where the error correction code is a Reed-Solomon error correction code.

13. (Previously Presented) A host computer, comprising:

a host memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and

a host processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory

sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer.

14. (Previously Presented) The host computer of claim 13, where the host processor executes instructions to replace addresses before the processor executes instructions to encode and decode data with the error correction code during data transfers.

15. (Previously Presented) The host computer of claim 13, where the host processor executes instructions to encode data with the error correction code before the host processor executes instructions to replace addresses during a write operation.

16. (Previously Presented) The host computer of claim 13, where the host processor executes instructions to provide sequential address data transfers between the storage device and the host computer.

17. (Original) The host computer of claim 16, where the sequential address data transfers are divided into sub-transfers around addresses of defective memory sections that are replaced with addresses of spare memory sections.

18. (Previously Presented) The host computer of claim 13, where the host memory stores instructions for a digital camera and the host processor executes the instructions to perform functions of the digital camera.

19. (Previously Presented) The host computer of claim 13, where the host memory stores instructions for a personal digital assistant and the host processor executes the instructions to perform functions of the personal digital assistant.

20. (Original) The host computer of claim 13, where the storage device comprises a magnetic random access memory.

21. (Original) The host computer of claim 13, where the storage device comprises a phase change random access memory.

22. (Original) The host computer of claim 13, where the storage device comprises a probe-based memory.

23. (Previously Presented) A host computer system, comprising:

means for correcting errors in data retrieved from a storage style memory device, the means for correcting errors comprising computer readable instructions stored in a host memory of the host computer system;

means for identifying defective sections of memory in the storage style memory device, where the defective sections of memory provide more errors than a predetermined threshold value; and

means for sparing the defective sections of memory with replacement sections of memory in the storage style memory device, the means for sparing comprising computer readable instructions stored in the host memory of the host computer system.

24. (Original) The computer system of claim 23, where the means for correcting errors comprises a multiple-bit per symbol error correction code.

25. (Original) The computer system of claim 23, where the means for correcting errors comprises a single-bit per symbol error correction code.

26. (Original) The computer system of claim 23, where the means for identifying comprises:

means for counting the number of errors in a selected section of memory in the storage style device;

means for comparing the number of errors to the predetermined threshold value to obtain a compare result; and

means for indicating if the selected section of memory is defective based on the compare result.

27. (Original) The computer system of claim 23, where the means for identifying comprises:

means for storing an address location of one of the defective sections; and

means for storing an address location of one of the replacement sections, where the address location of one of the replacement sections corresponds to the address location of one of the defective sections.

28. (Previously Presented) The computer system of claim 27, where the means for sparing comprises means for replacing the address location of one of the defective sections with the corresponding address location of one of the replacement sections during data transfers between the host computer system and the storage style memory device.

29. (Previously Presented) A method for storing and retrieving data, comprising:

providing a host computer and a memory device;

providing computer-executable sparing instructions and error correction code instructions;

replacing addresses for defective memory sections in a memory device with addresses for replacement memory sections in the memory device by executing the sparing instructions on the host computer;

providing the addresses for the replacement memory sections to the memory device during read and write operations with the memory device by executing the sparing instructions on the host computer;

encoding original data with an error correction code to write encoded data into the memory device by executing the error correction code instructions on the host computer; and

decoding data retrieved from a selected memory section of the memory device with the error correction code by executing the error correction code instructions on the host computer.

30. (Original) The method of claim 29, comprising:

maintaining a table of the addresses for defective memory sections and the addresses for replacement memory sections; and

searching the table to match original addresses with the addresses for defective memory sections.

31. (Original) The method of claim 29, comprising:

updating a table with new addresses for defective memory sections; and

assigning new addresses for replacement memory sections that correspond with the new addresses for defective memory sections.

32. (Original) The method of claim 29, comprising:

counting errors in the data retrieved from the selected memory section to obtain an error count;

comparing the error count to error correction capabilities of the error correction code; and

indicating the selected memory section is defective if the number of errors exceeds a predetermined portion of the error correction capabilities.

33. (Original) A method for storing and retrieving data, comprising:

providing a host computer and a storage style memory device;

providing computer-executable sparing instructions and error correction code instructions;

sparing out sections of memory in the storage style memory device by executing the sparing instructions on the host computer; and

encoding and decoding data stored in the storage style memory device with an error correction code by executing the error correction code instructions on the host computer.

34. (Original) The method of claim 33, comprising:

detecting grown defective sections of memory in the storage style memory device; and

sparing out the detected grown defective sections of memory.

35. (Original) The method of claim 33, comprising:

encoding only selected data; and

decoding only the encoded data stored in the storage style memory device.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.